1. An apparatus for writing a target address of a taken branch instruction into a branch target address cache (BTAC) upon execution of the taken branch instruction, the BTAC having a plurality of storage elements for caching target addresses of executed branch instructions, each of the plurality of storage elements comprising first and second entries for storing a target address, the apparatus comprising:

a global indicator, for specifying a global one of the first and second entries of the BTAC plurality of storage elements; and

branch control logic, coupled to said global indicator, for selecting one of the first and second entries to write the taken branch instruction target address into based on said global indicator.

2. The apparatus of claim 1, wherein said global one of the first and second entries specifies which of the first and second entries was last written to in any one of the plurality of storage elements when both of the first and second entries therein were invalid.

3. The apparatus of claim 2, wherein said branch control logic selects an opposite of said global one of the first and second entries specified in said global indicator to write the taken branch instruction target address into.

4. The apparatus of claim 3, wherein said branch control logic updates said global indicator to specify said selected entry.

5. The apparatus of claim 4, wherein said branch control logic updates said global indicator in conjunction with the BTAC writing the taken branch instruction target address into said selected entry.

6. The apparatus of claim 4, wherein the plurality of storage elements also includes a valid indicator associated with each of the first and second entries, for indicating whether the target address stored therein is valid or invalid.

7. The apparatus of claim 6, wherein said branch control logic selects one of the first and second entries based on said global indicator only if said associated valid indicators indicate both of the first and second

entries are invalid in one of the plurality of storage elements that is selected for updating.

8. The apparatus of claim 6, wherein if only one of the first and second entries is invalid in one of the plurality of storage elements that is selected for updating, said branch control logic selects said invalid entry to write without regard to said global indicator.

9. The apparatus of claim 6, wherein the BTAC comprises a least recently used indicator associated with each of the plurality of storage elements for indicating which of the first and second entries in said associated storage element was least recently used.

10. The apparatus of claim 9, wherein if both of the first and second entries are valid in one of the plurality of storage elements that is selected for updating, said branch control logic selects one of said valid first and second entries to write based on said least recently used indicator without regard to said global indicator.

11. The apparatus of claim 6, wherein said branch control logic updates said global indicator only if both of

the first and second entries are invalid in one of the plurality of storage elements that is selected for updating.

12. The apparatus of claim 1, wherein the BTAC selects one of the plurality of storage elements for writing the taken branch instruction target address to based on an instruction pointer of the taken branch instruction.

13. An apparatus for writing a target address in a branch target address cache upon execution of a taken branch instruction, comprising:

a branch target address cache (BTAC), comprising a plurality of storage elements for caching target addresses of executed branch instructions, each of said plurality of storage elements comprising first and second entries for storing a target address;

a global indicator, configured to store a global indication of which of said first and second entries was last written to in any of said plurality of storage elements when at least one of said first and second entries were invalid in a last written one of said plurality of storage elements; and

branch control logic, coupled to said global indicator, for selecting which of said first and second entries to write the taken branch instruction target address to based on said global indicator.

14. A method for replacing a target address in a branch target address cache (BTAC) having a plurality of storage locations each having an A and B entry for caching a target address, the method comprising:

executing a branch instruction and generating a target address thereof;

selecting one of the plurality of storage locations of the BTAC based on an instruction pointer of said branch instruction;

determining whether both the A and B entries of said selected BTAC storage location are invalid;

examining a replacement status flag shared globally by the plurality of BTAC storage locations; and

writing said target address to one of the A and B entries of said selected BTAC storage location based on said replacement status flag if both the A and B entries of said selected BTAC storage location are invalid.

15. The method of claim 14, wherein said determining whether both the A and B entries of said selected BTAC storage location are invalid comprises examining a

valid status indicator associated with each of the A and B entries comprised in said selected BTAC storage location.

16. The method of claim 14, wherein said examining said replacement status flag comprises determining which of the A and B entries was last written to by a write to any of the plurality of storage locations in which both the A and B entries were invalid.

17. The method of claim 16, wherein said writing said target address comprises writing to one of the A and B entries not last written to as indicated by said replacement status flag.

18. The method of claim 14, wherein said examining said replacement status flag comprises determining which of the A and B entries was last written to by a write to any of the plurality of storage locations in which at least one of the A and B entries was invalid.

19. The method of claim 18, wherein said writing said target address comprises writing to one of the A and B entry not last written to as indicated by said replacement status flag.

20. The method of claim 14, further comprising:

determining if only one of the A and B entries of said selected BTAC storage location is invalid; and

writing said target address to said invalid one of the A and B entries of said selected BTAC storage location if only one of the A and B entries is invalid.

21. The method of claim 14, further comprising:

determining if both of the A and B entries of said selected BTAC storage location are valid; and

writing said target address to one of the A and B entries of said selected BTAC storage location based on a replacement status flag associated with said selected BTAC storage location.

22. The method of claim 21, wherein said writing said target address to said one of the A and B entries of said selected BTAC storage location based on said replacement status flag associated with said selected BTAC storage location comprises writing to said one of the A and B entries least recently used as indicated by said replacement status flag associated with said selected BTAC storage location.

23. A method for replacing a target address in a branch target address cache (BTAC) having a plurality of storage locations each having N entries for caching a target address, wherein N is an integer greater than one, the method comprising:

executing a branch instruction and generating a target address thereof;

selecting one of the plurality of storage locations of the BTAC based on an instruction pointer of said branch instruction;

determining whether all of the N entries of said selected BTAC storage location are invalid;

examining a replacement status flag shared globally by the plurality of BTAC storage locations; and

writing said target address to one of the N entries of said selected BTAC storage location based on said global replacement status flag if all of the N entries of said selected BTAC storage location are invalid.

24. The method of claim 23, wherein said examining said global replacement status flag comprises determining

which of the N entries was least recently written to among writes to any of the plurality of storage locations wherein all N entries were invalid.

25. The method of claim 24, wherein said writing said target address comprises writing to said one of the N entries least recently written to as indicated by said global replacement status flag.

26. A pipelined microprocessor, comprising:

a branch target address cache (BTAC), comprising a plurality of lines each having N target addresses stored therein, N being an integer greater than one;

execution logic, coupled to said BTAC, configured to execute a branch instruction and generate a target address thereof for storage in said BTAC;

address selection logic, coupled to said BTAC, configured to select an instruction pointer of said executed branch instruction for updating said BTAC;

a status register, coupled to said execution logic, for storing replacement status global to said plurality of BTAC lines; and

branch control logic, configured to select, for replacing with said branch instruction target address, one of said N target addresses that are stored in one of said plurality of lines selected by said instruction pointer, said branch control logic configured to select said one of said N target addresses as a function of said global

replacement status stored in said status register.

27. The microprocessor of claim 26, further comprising:

an instruction cache, indexed by a fetch address;

wherein said address selection logic selects said fetch address for reading said BTAC.

28. The microprocessor of claim 26, wherein said branch control logic is configured to select for replacing one of said N target addresses stored in said selected line as a function of said global replacement status only if all of said N target addresses that are stored in said selected line are invalid.

29. The microprocessor of claim 28, wherein said control logic selects a least recently written one of said N target addresses among previous writes to ones of said plurality of lines that has all N invalid target addresses.

30. The microprocessor of claim 28, wherein said control logic selects a least recently written one of said N target addresses among previous writes to ones of said

plurality of lines that has at least one invalid target address.

31. The microprocessor of claim 26, wherein said branch control logic is configured to select for replacing one of said N target addresses stored in said selected line as a function of said global replacement status only if more than one of said N target addresses that are stored in said selected line are invalid.

32. The microprocessor of claim 31, wherein said control logic selects a least recently written one of said N target addresses among previous writes to ones of said plurality of lines that has more than one invalid target address.